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ABSTRACT

In a manufacturing process of a semiconductor integrated circuit device having an inlaid interconnect structure by embedding a conductor film in a recess 4 such as trench or hole formed in an organic insulating film 2 which constitutes an interlevel dielectric film and includes an organosiloxane as a main component, the recess 4 such as trench or hole is formed by subjecting the organic insulating film 2 to plasma dry etching in a CF₃-based gas/N₂/Ar gas in order to suppress the formation of an abnormal shape on the bottom of the recess 4, upon formation of a photoresist film 3 over the organic insulating film 2, followed by formation of the recess 4 therein with the photoresist film 3 as an etching mask.